Chiplet Integration by Die-to-Die Pillar-Suspended Bridge

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Abstract

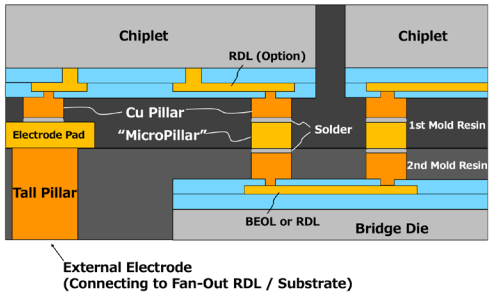
Chiplet integration technology, which has the potential to scalable expand capabilities by integrating many integrated circuit (IC) chips with different manufacturing processes, structures, and functions while maintaining the data transfer bandwidth between IC chips, is attracting attention as a promising method to solve the problems such as slowdown of Moore's law and the von Neumann bottleneck. Die-to-die bridge structures that connect dies via locally placed bridge chips with high-density interconnects is expected for scalable chiplet integration. We proposed novel die-to-die bridge architecture called "Pillar-Suspended Bridge (PSB)" that connects between chiplet and bridge via "MicroPillars" in molded form using panel-level manufacturing process. We successfully demonstrated proof-of-concept (PoC) through prototyping chiplets/bridge integrated module with 40 μm pitch MicroPillars using 300 mm × 300 mm panel-level manufacturing process. We confirmed fine-pitch die-to-die connection with MicroPillars and 20 μm thick bridge die by cross-sectional analysis of the module. We also evaluated warpage behavior of the PSB module in the reflow temperature range using shadow moiré method and confirmed warpage of less than 10 μm. Finally, we discussed scalability of this technology including external connections for Fan-Out RDL and optics.

Key words

Chiplet, Integration, Die-to-Die, Bridge, Interconnect

I. Introduction

For applications such as artificial intelligence (AI) and metaverse, which require huge computing power, the limitations of conventional semiconductor IC technology and computer architecture, such as the slowdown of Moore's law and the von Neumann bottleneck, are becoming serious problem. In response, chiplet integration technology, which has the potential to scalable expand capabilities by integrating many IC chips with different manufacturing processes, structures, and functions while maintaining the data transfer bandwidth between IC chips, is attracting attention as a promising method to solve such problems. Chiplet integration platform technologies including silicon interposer and redistribution layer (RDL) interposer have scalability to wafer size, but they have difficulty to scaling more large panel size while maintaining high-density wiring. In contrast, bridge structures that connect via locally placed bridge chips with high-density interconnects may solve these scalability issues. Some bridge structures and processes have been proposed and developed, but their chiplet-to-bridge connection accuracy, scalability, and cost would be issues because of their process complexity. In this report, we



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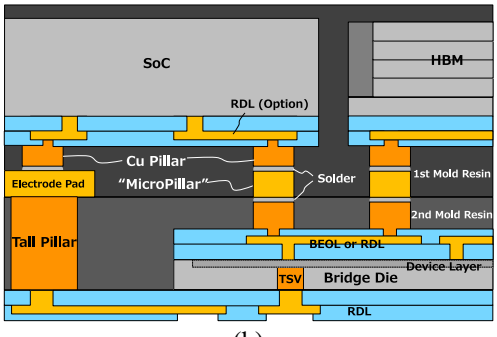


(b)

Fig. 1 "Pillar Suspended Bridge" architecture; (a) basic structure; (b) variations

propose novel die-to-die bridge architecture that connects between chiplet and bridge via “MicroPillars” in molded form using large area panel-level manufacturing process.

II. Bridge Architecture using MicroPillar

A. Conventional Architecture

The bridge connection structure currently proposed mainly consists of a bridge with high-density wiring embedded inside a printed circuit board (PCB) or redistribution layer (RDL) using the so-called "Chip-first" method, followed by the connection of chiplets via the high-density wiring of the bridge [1], [2]. In this case, the positioning accuracy of the embedded bridge depends on the accuracy of the low face-up type die bonder, and it is degraded by stress during resin encapsulation called "Die shift". This process also makes it difficult to make the bridge die thinner. Furthermore, since the wiring layer is formed after the bridge is mounted, there are concerns about yield loss, especially when manufacturing large panels.

On the other hand, a type of structure that directly connects chiplets and bridges with bumps without such a wiring layer has been proposed [3], but there are many concerns in terms of productivity, reliability, and scalability of chiplet integration.

B. Proposed Architecture

In this study, we devised a bridge connection structure that applies the chip-last method, which does not have the chip positioning accuracy problems inherent in the chip-first method, to both chiplets and bridges, and does not require complex processes such as wiring layer formation after the connection of these components (“All Chip-last” method).

Fig. 1 shows the bridge connection structure based on the proposed "Pillar-Suspended Bridge (PSB)" structure [4]. Only a metal pillar called a "MicroPillar" exists at the connection between the chiplet and bridge, and Cu pillar electrodes of the chiplet and bridge are connected above and below it. The chiplet and bridge sides are molded and sealed with resin, and the mold resin is in contact with each other. An external electrode called a "Tall Pillar" is formed through the mold on the bridge side.

The chiplet-to-chiplet interconnects in the bridge can be sub-micron to a few μm in width using the Back End of Line (BEOL) damascene method in the normal Si wafer process, or RDL with polymer interlayer dielectrics, which has excellent high-frequency transmission characteristics. The BEOL bridge and RDL bridge can be used in a single chiplet integrated module for performance optimization. RDLs can also be formed on the chiplet for power supply and signal electrode relocation.

Proposed chiplet integrated module can be assembled into conventional package like Flip Chip-Ball Grid Array (FC-BGA), Fan-Out, or wire-bonded packages because of its simple structure with minimum components.

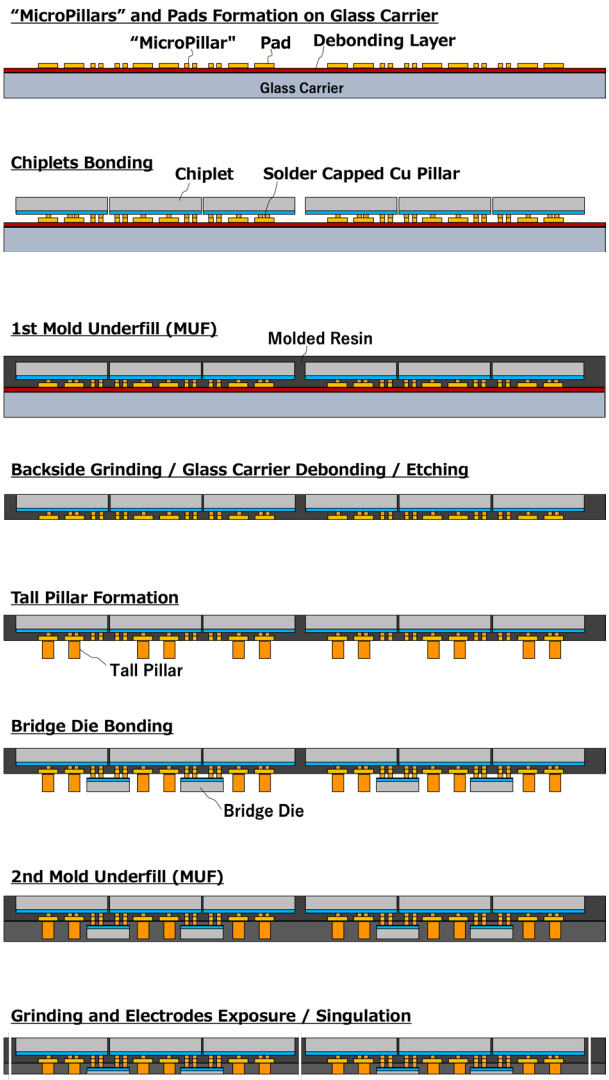


Fig. 4 Fabrication process flow of PSB

III. Manufacturing Process and Prototyping

A prototype of the proposed PSB structure was manufactured for Proof of Concept (PoC). The prototype process flow is shown in Fig. 4.

MicroPillar and electrode pads were formed by semi-additive process (SAP) on a 300 mm × 300 mm panel glass carrier with debonding/seed layers first. The pitch of the MicroPillar was 40 μm, and the pitch of the electrode pad was 142 μm. The MicroPillar and electrode pads were formed by a semi-additive process (SAP). Chiplets with SnAg capped Cu pillar electrodes and RDL were bonded to the top of the MicroPillar and electrode pads using a flip chip bonder. Fig. 5 shows Scanning Electron Microscope (SEM) image of the Cu pillar electrode of the chiplets. Thermo-compression bonding (TCB) was used as the bonding

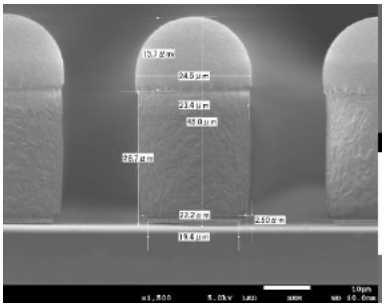
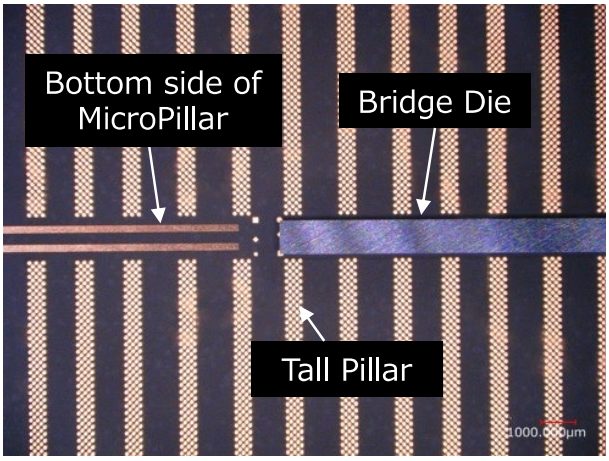


Fig. 5 Cu pillar bump on chiplet/bridge

method. In this process, side walls of MicroPillars were covered by native oxide of metals, so solder wetting to side walls and its undesirable effects were prevented. The chiplets were 9.96 mm × 7.06 mm and 720 µm thick. The chiplets were designed as two chips connected in pairs, with a chip spacing of 200 µm. The entire chiplet were sealed using a panel-level Mold Underfill (MUF) process. We used granule resin and molding temperature was 140°C in this process. Chiplets-to-carrier gap underfilling of 40 µm pitch Cu pillar/MicroPillar connection were successfully demonstrated without voids thanks to their sufficient total gap. Following mechanical grinding of the chiplet side of the panel, mechanical debonding of the glass carrier from molded chiplets panel was carried out. After etching of the seed layer on the debonded surface, the MicroPillars and electrode pads embedded in the mold resin were exposed.

On the above exposed electrode pad, a 100 µm high Cu pillar called "Tall Pillar" was formed by the SAP method. Electroless plating of antioxidant metallization including Au layer on exposed bottom side of MicroPillars were executed. Debonded resin panel with embedded chiplets was almost no warping because it had no layer structure with different coefficient of thermal expansion (CTE). We conducted very stable bridge die bonding spanning over two chiplets on this very flat surface which has CTE close to silicon because of embedded chiplets. The bridge die was 9.96 mm × 0.96 mm and 200 µm thick. The bridge dies had also 40 µm pitch solder capped Cu pillar bumps and they were bonded on exposed bottom side of MicroPillars with antioxidant metallization. Fig. 6 shows (a) top view and (b) oblique view of bridge die bonded on embedded chiplets. Tall pillars are also shown close to the bridge die. Following bridge die bonding process, second MUF process was performed over the Tall Pillars and bridge dies. They encapsulated not only bridge dies but also gap of bridge dies and resin panel perfectly. Mechanical grinding on the bridge die side was executed, and bridge dies were thinned to about 20 µm. Tall Cu Pillars were also exposed on molded surface of bridge die side, and they formed external terminals of this chiplet integrated module. Fig. 7 shows Appearance of thinned bridge and exposed Tall Pillars after molding/grinding.



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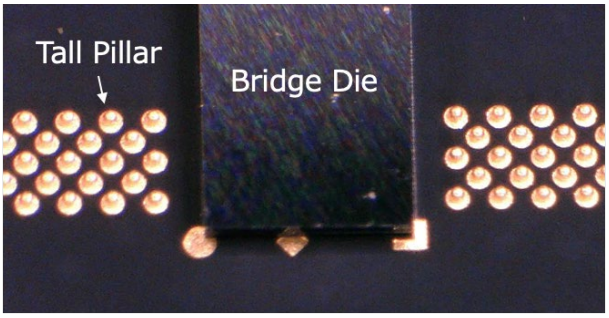


(b)

Fig. 6 External view of the bridge bonded on embedded chiplets; (a) top view; (b) oblique view

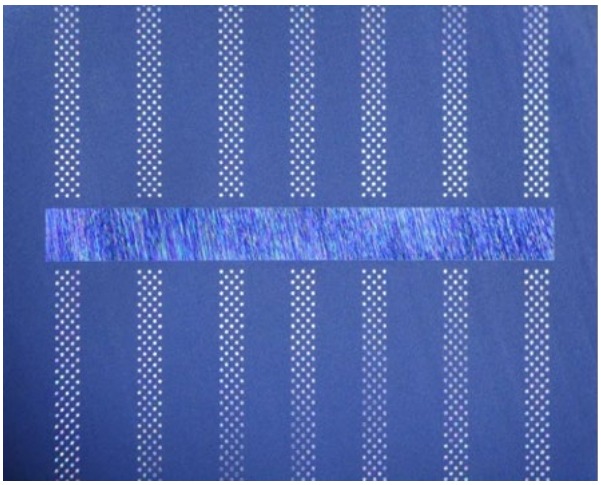


Fig. 7 Appearance of thinned bridge and exposed Tall Pillars after molding/grinding

Finally, the panel was diced with a blade to complete a 10.60 mm × 14.94 mm chiplet integrated module consisting of two chiplets and one bridge.

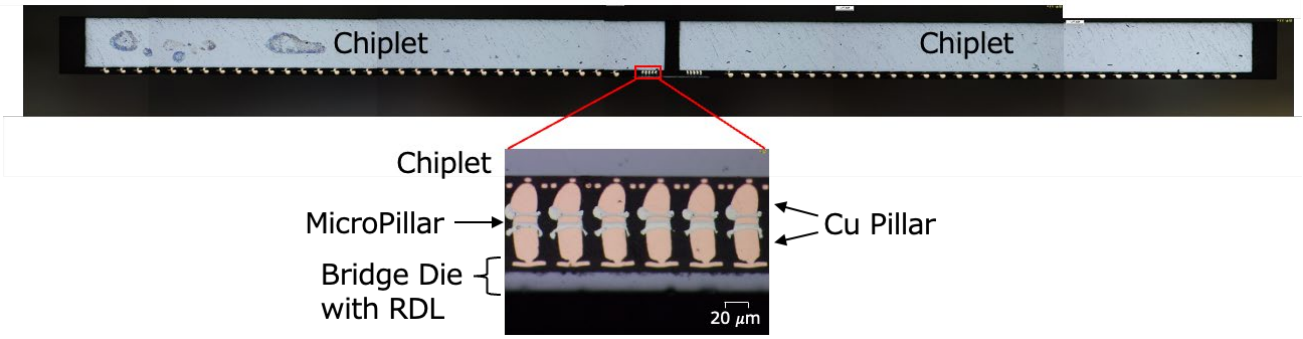


Fig. 8 Cross-sectional view of PSB proof-of-concept sample

IV. Prototype Sample Analysis

A. Cross-sectional Analsis

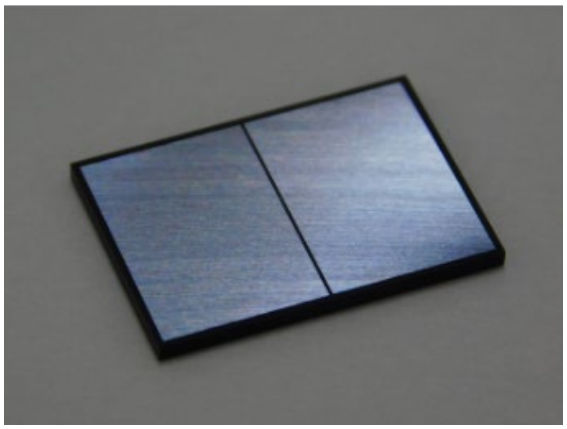
Fig. 8 shows a cross-sectional view of the PoC sample in the direction of the inter-chiplet connection via bridge, and Fig. 9 shows an external view of the PoC sample. The cross-sectional structure of Fig. 8 shows that the chiplets and bridges are realized with the expected structure, that the chips are connected with each pillar electrode/MicroPillar, and that the Si thickness of the bridge is about 20 μm.

B. Warpage Analsis

Warpage characteristics is very important for chiplet/bridge assembly process and assembly PSB with interposer.

We measured the warpage behavior of the PSB module in the reflow temperature range. Fig. 10 shows the warpage measurement results of the PSB chiplet integrated module using the shadow moiré method. The positive direction is convex and warped when viewed from the chiplet side. This may be due to curing and thermal shrinkage of the resin on the bridge surface. At room temperature, convex warping of about 4 μm is observed. The direction of warpage reversed as the temperature increased, and at a reflow temperature of about 260°C, the warpage was about 7 μm concave.

These values of warpage appear small, but we need to further reduce these values. When bonding the bridge, the molded panel in which the chiplets are embedded must be as flat as possible and the CTE must be consistent with Si. Furthermore, the warpage of the PSB module must be as small as possible when connecting the huge chiplet integrations to external systems. We can address these objectives by controlling the mold resin thickness, especially the overmold thickness on the back side of the chiplets.



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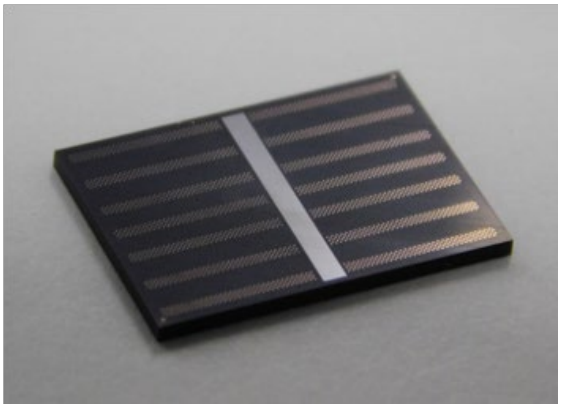

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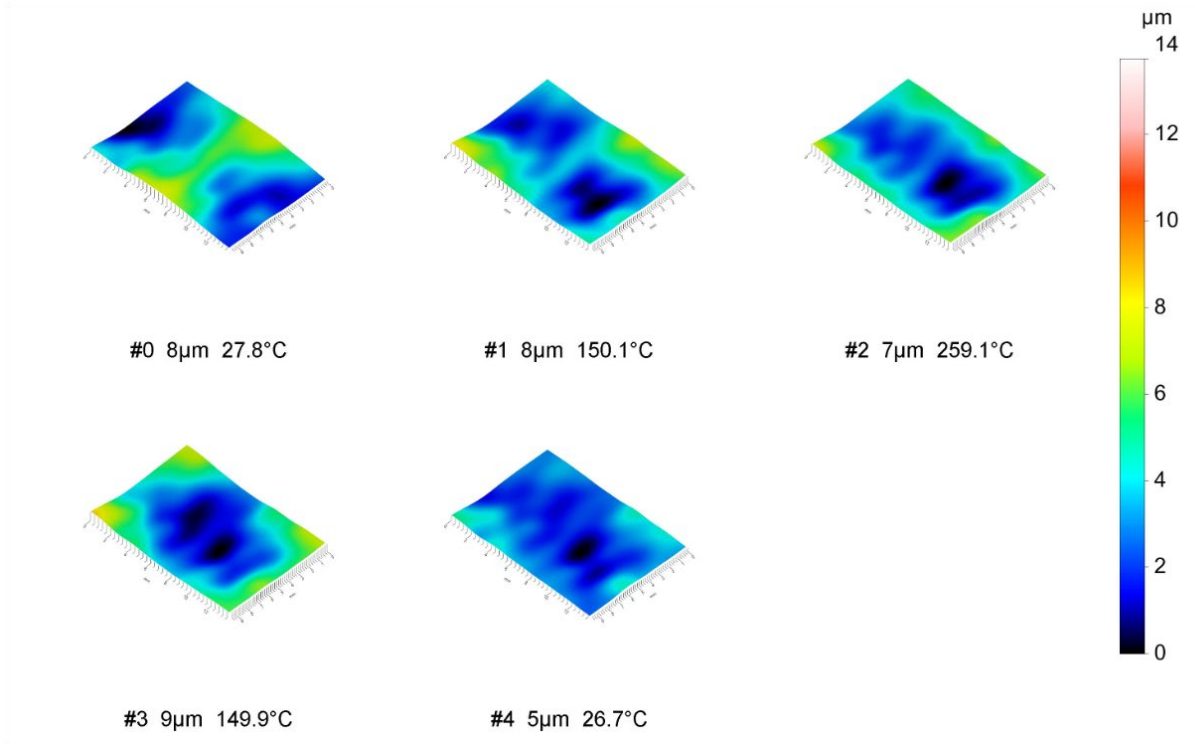
Fig. 9 External view of PSB proof-of-concept sample; (a) chiplet side and (b) bridge/electrode side



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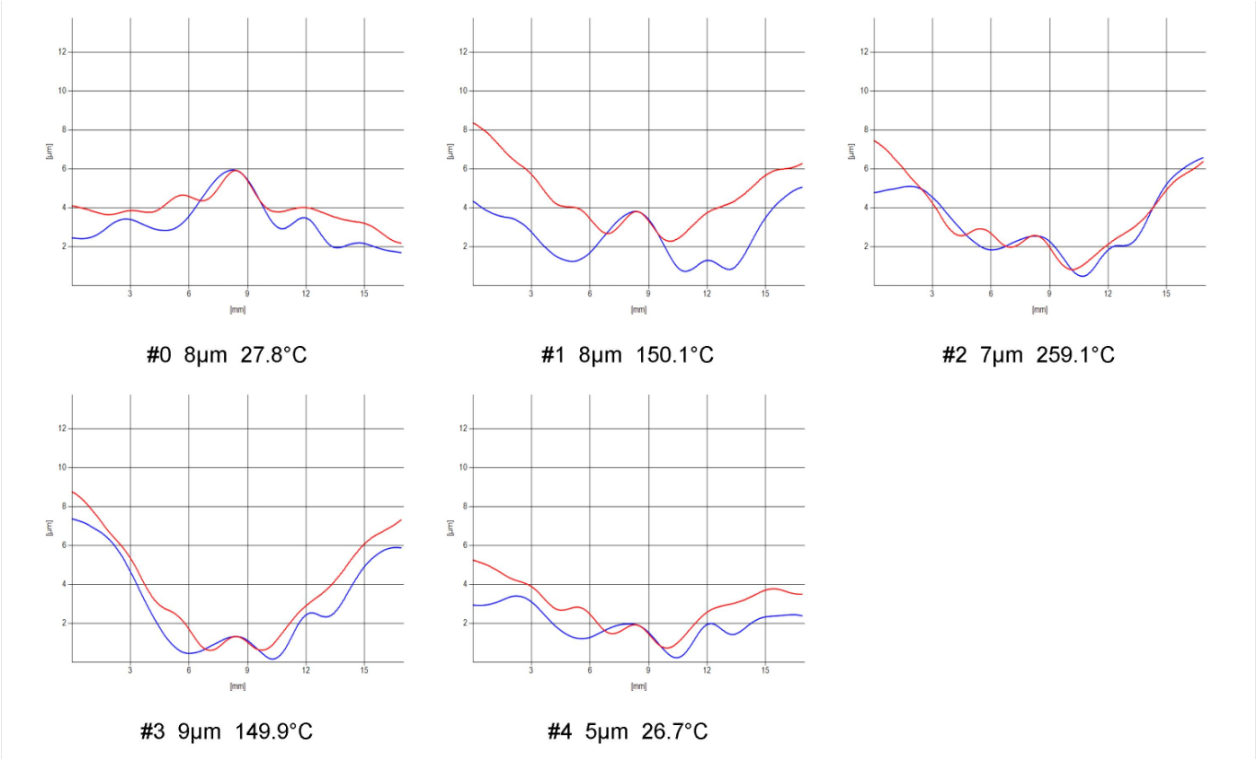

(b)

Fig. 10 Warpage behavior of the PSB module in the reflow temperature range; (a) 3D plots; (b) diagonals

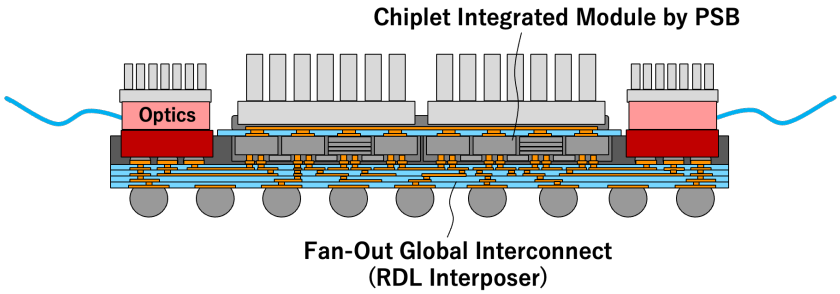

Fig. 11 PSB chiplet integrated module with Fan-Out interconnect

V. Consideration

The most important factors contributing to the realization of this concept are (1) high bonding accuracy and suppression of "die shift" during the process by the "All Chip-last" process and (2) a bonding process consistent with the CTE [5], [6]. For (1), the bonding/fixation of the chiplet and bridge using the MicroPillar formed on the carrier glass as a common mediator. For (2), the bonding of the chiplet to the glass carrier, which has a linear expansion similar to that of Si, and the bonding of the bridge to the panel in which the chiplets are embedded. The absence of resin layers with high CTE other than the mold resin also contributes to the suppression of panel warpage during the process. The combination of these factors is believed to be responsible for the highly accurate joining of the chiplet/bridge.

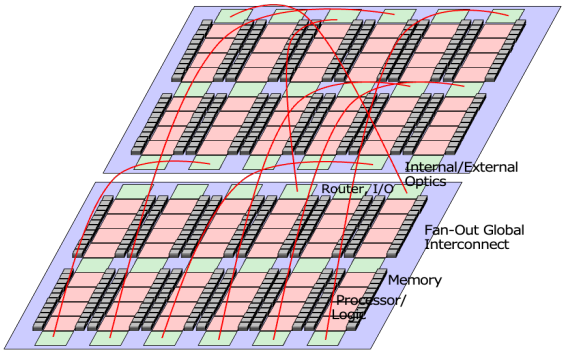

Fig. 12 Extreme large-scale chiplet integration

VI. Conclusion

PSB was devised as a minimum-element chiplet integration structure/process, and a prototype PoC was conducted to prove its feasibility.

Structurally, the minimal chiplet/bridge connection structure is expected to improve chip-to-chip connection density and electrical characteristics, and the thin bridge is expected to improve electrical characteristics/heat dissipation performance from the chiplet to the outside. In addition, it has the advantages of selectable bridge wiring types, no yield problems when expanding the scale of integration (Known Good Bridge), and the ability to scale the size of integrated modules.

By connecting a wiring layer with fan-out function (e.g., RDL Interposer) to the PSB structure, an ideal chiplet-integrated package as shown in Fig. 11, or an extreme large-scale chiplet integration as shown in Fig. 12 could be realized.

We believe demonstrated die-to-die interconnection architecture with pillar-suspended bridge will provide realistically the simplest structure and processes for scalable chiplet integration because there are no complicated processes after assembly, and it enables extreme large-scale integration while controlling yield problem.

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